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Minamoto et al.

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(45) **Date of Patent: Apr. 26, 2016**

(54) **SEMICONDUCTOR MEMORY DEVICE WITH MEMORY CELLS EACH INCLUDING A CHARGE ACCUMULATION LAYER AND A CONTROL GATE**

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(30) **Foreign Application Priority Data**

Jan. 30, 2009 (JP) 2009-019678

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G11C 16/08 (2006.01)
H01L 27/115 (2006.01)
G11C 16/04 (2006.01)

(52) **U.S. Cl.**
CPC ***G11C 16/08*** (2013.01); ***G11C 16/0483*** (2013.01); ***H01L 27/11519*** (2013.01)

(58) **Field of Classification Search**
CPC G11C 5/025; G11C 5/06; G11C 5/063; G11C 16/08; G11C 16/0483; H01L 27/11519; H01L 27/11526; H01L 27/11529; H01L 27/11565; H01L 27/11573
See application file for complete search history.

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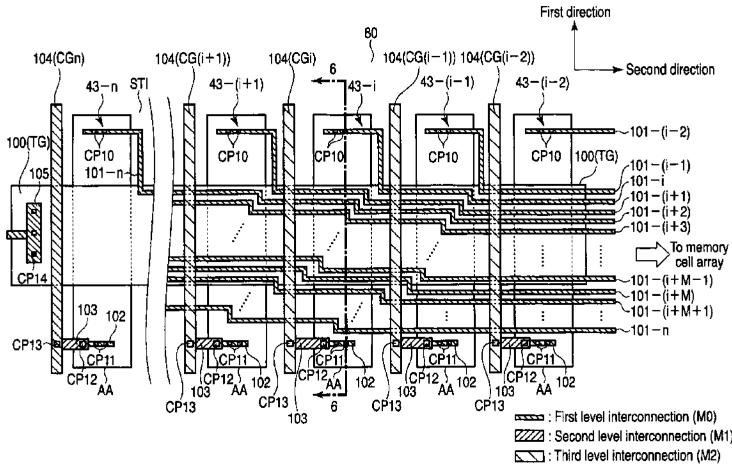
(57) **ABSTRACT**

A semiconductor memory device includes a memory cell unit, word lines, a driver circuit, and first transistors. The word lines are connected to the control gates of 0-th to N-th memory cells. The (N+1) number of first transistors transfer the voltage to the word lines respectively. Above one of the first transistors which transfers the voltage to an i-th (i is a natural number in the range of 0 to N) word line, M (M<N) of the word lines close to the i-th word line pass through a region above the gate electrode by a first level interconnection without passing over the impurity diffused layers.

6 Claims, 14 Drawing Sheets



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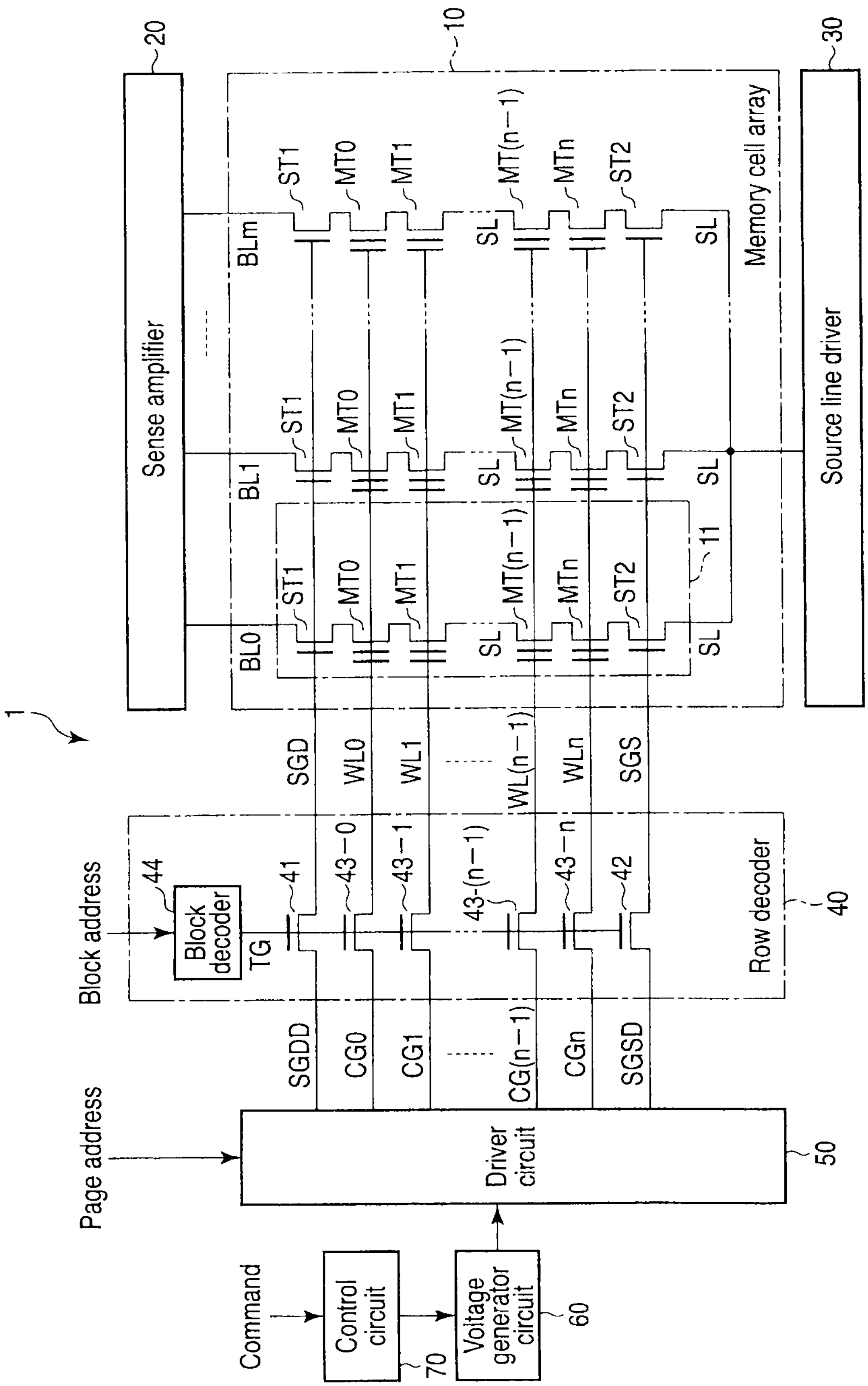
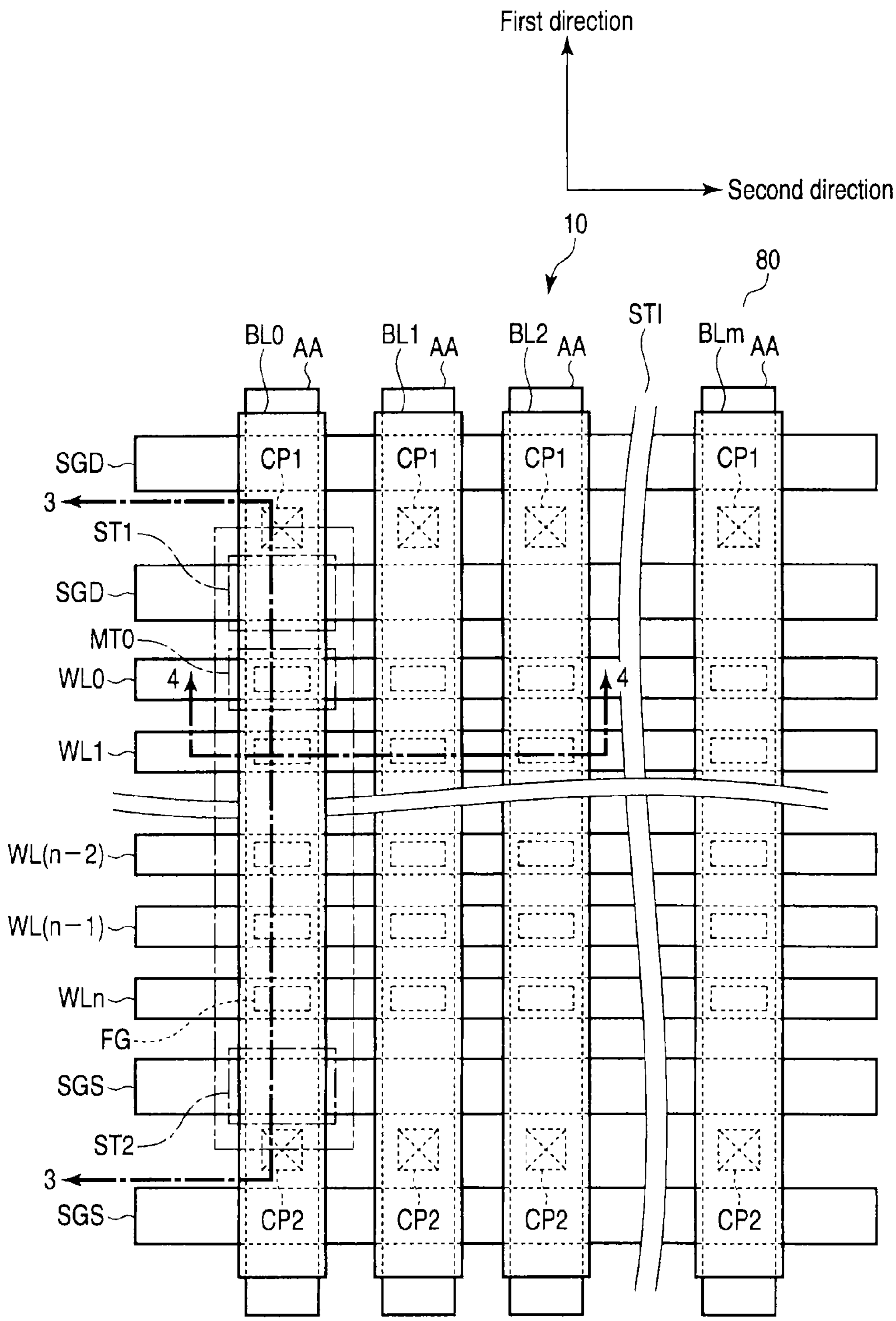
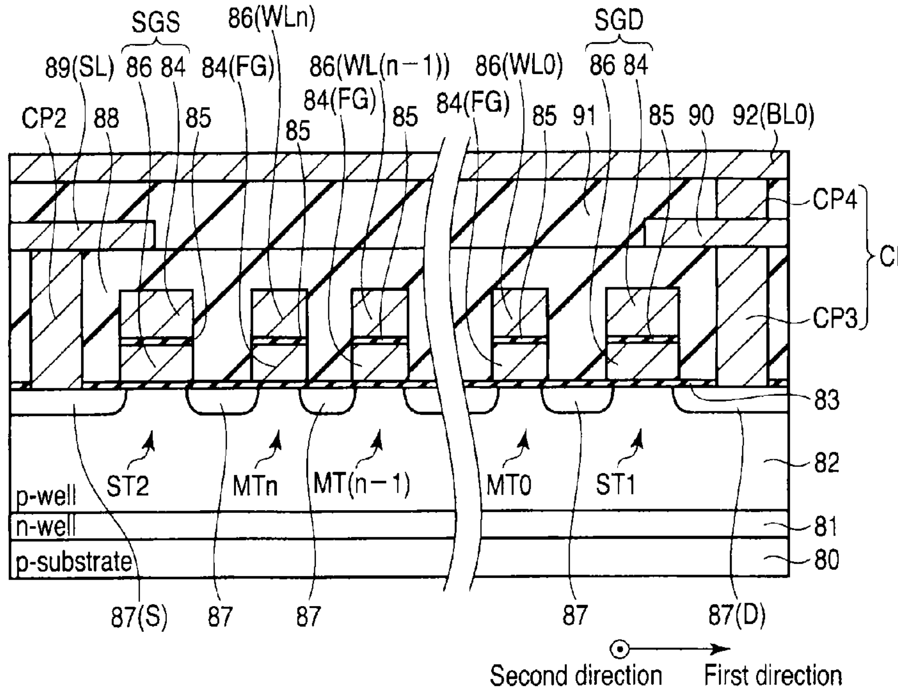

1
20
Sense amplifier
10
Memory cell array
30
Source line driver
BL0
BL1
BLm
ST1
MT0
MT1
MT(n−1)
MTn
ST2
SL
11
SGD
WL0
WL1
WL(n−1)
WLn
SGS
Block address
44
Block decoder
TG
41
43−0
43−1
43-(n−1)
43−n
42
Row decoder
40
SGDD
CG0
CG1
CG(n−1)
CGn
SGSD
Page address
Driver circuit
50
Command
Control circuit
70
Voltage generator circuit
60

F I G. 1

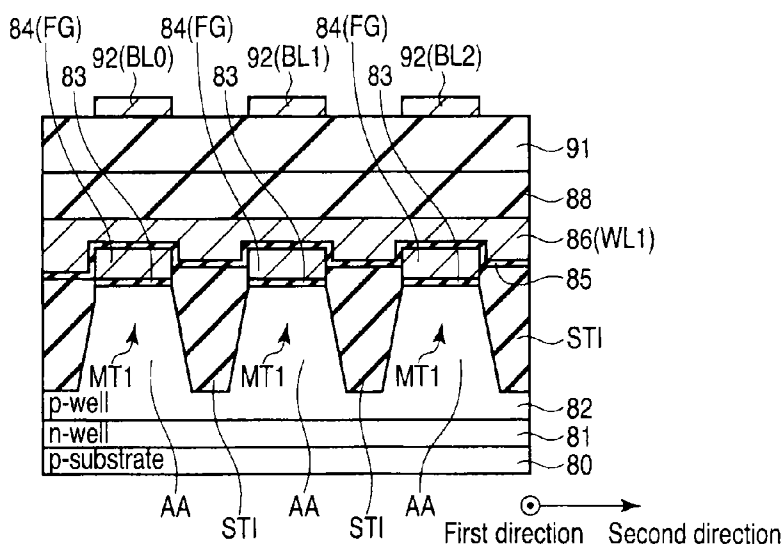

First direction
Second direction
10
80
STI
BL0
AA
BL1
AA
BL2
AA
BLm
AA
SGD
CP1
CP1
CP1
CP1
3
ST1
SGD
MT0
WL0
4
4
WL1
WL(n−2)
WL(n−1)
WLn
FG
SGS
ST2
3
SGS
CP2
CP2
CP2
CP2

F I G. 2



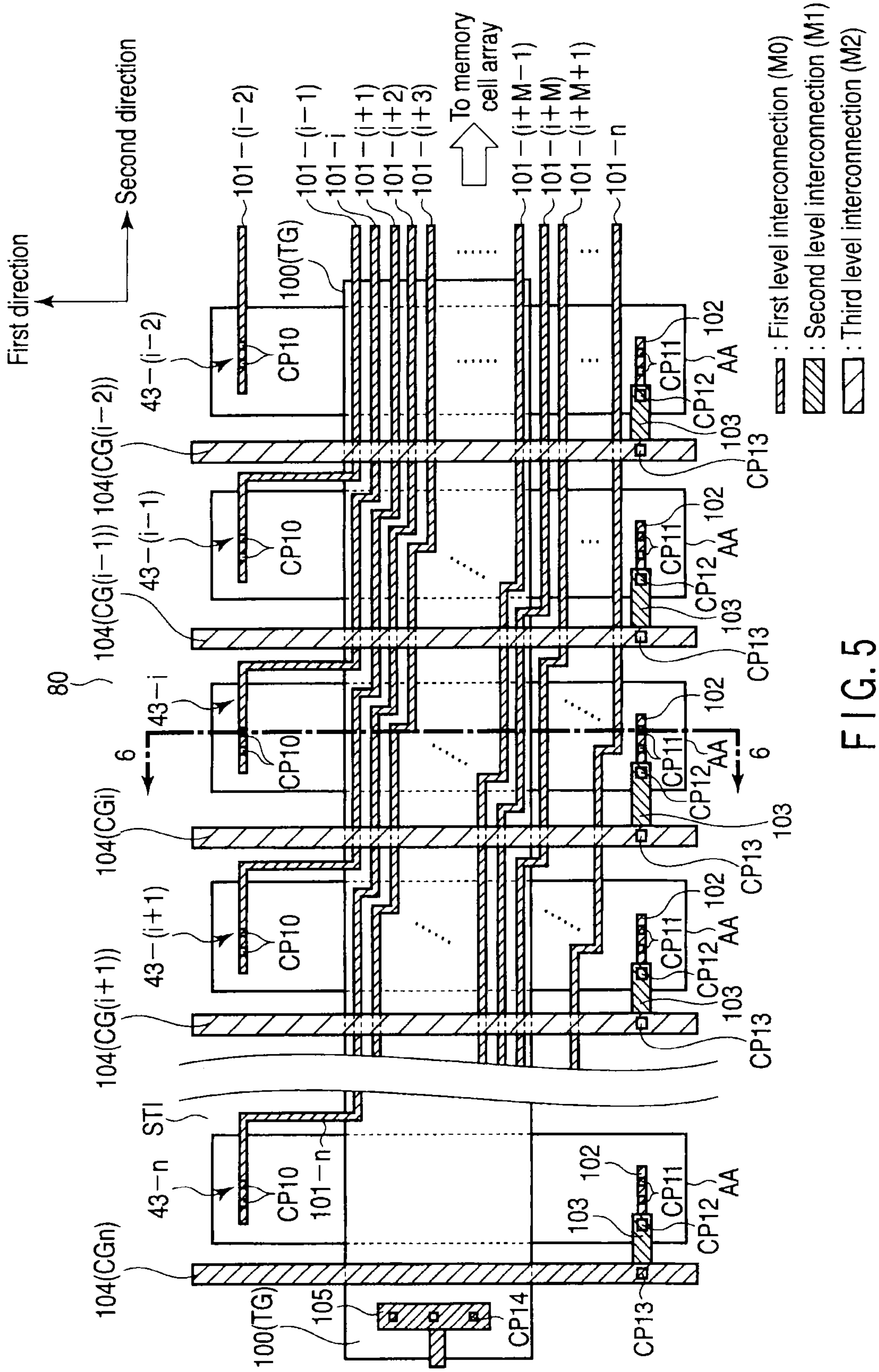
SGS
86(WLn)
SGD
89(SL)
86 84
84(FG)
86(WL(n−1))
86(WL0)
86 84
84(FG)
84(FG)
CP2
88
85
85
85
85
91
85
90
92(BL0)
CP4
CP1
CP3
83
82
81
80
p-well
ST2
MTn
MT(n−1)
MT0
ST1
n-well
p-substrate
87(S)
87
87
87
87(D)
Second direction
First direction

F I G. 3



84(FG)
84(FG)
84(FG)
92(BL0)
92(BL1)
92(BL2)
83
83
83
91
88
86(WL1)
85
STI
MT1
MT1
MT1
p-well
82
n-well
81
p-substrate
80
AA
STI
AA
STI
AA
First direction
Second direction

F I G. 4


First direction
Second direction
80
To memory cell array
101−(i−2)
101−(i−1)
101−i
101−(i+1)
101−(i+2)
101−(i+3)
101−(i+M−1)
101−(i+M)
101−(i+M+1)
101−n
100(TG)
43−(i−2)
43−(i−1)
43−i
43−(i+1)
43−n
CP10
CP11
CP12
CP13
CP14
102
103
105
AA
STI
6
104(CG(i−2))
104(CG(i−1))
104(CGi)
104(CG(i+1))
104(CGn)
: First level interconnection (M0)
: Second level interconnection (M1)
: Third level interconnection (M2)

F I G. 5

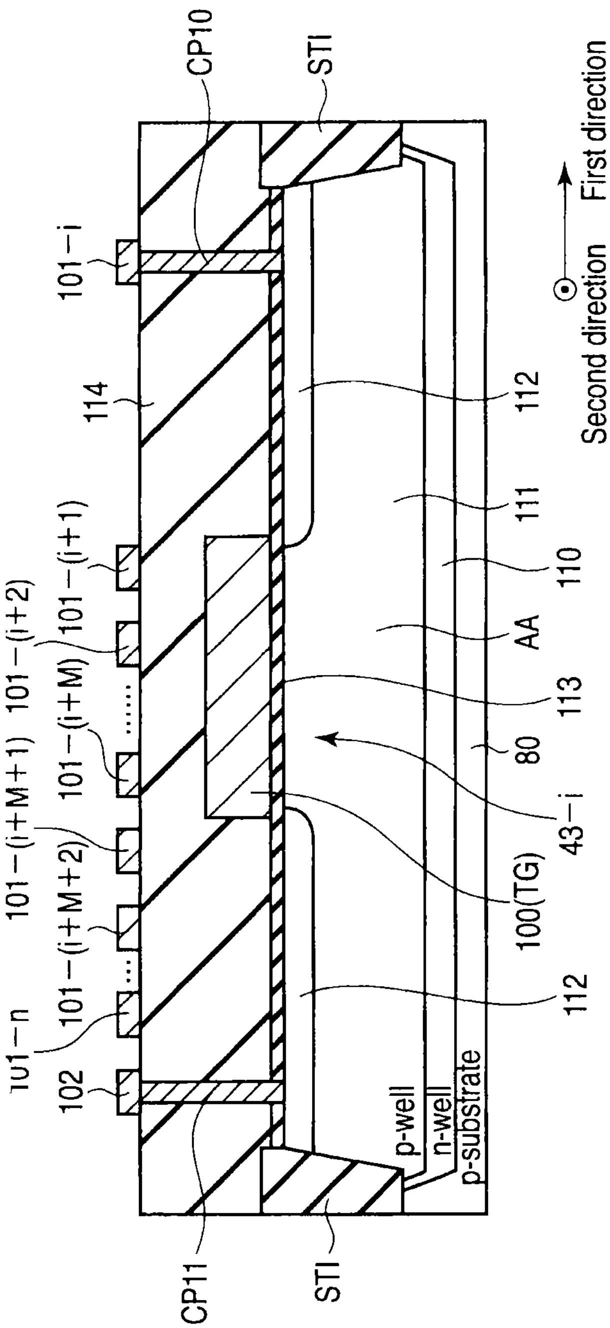
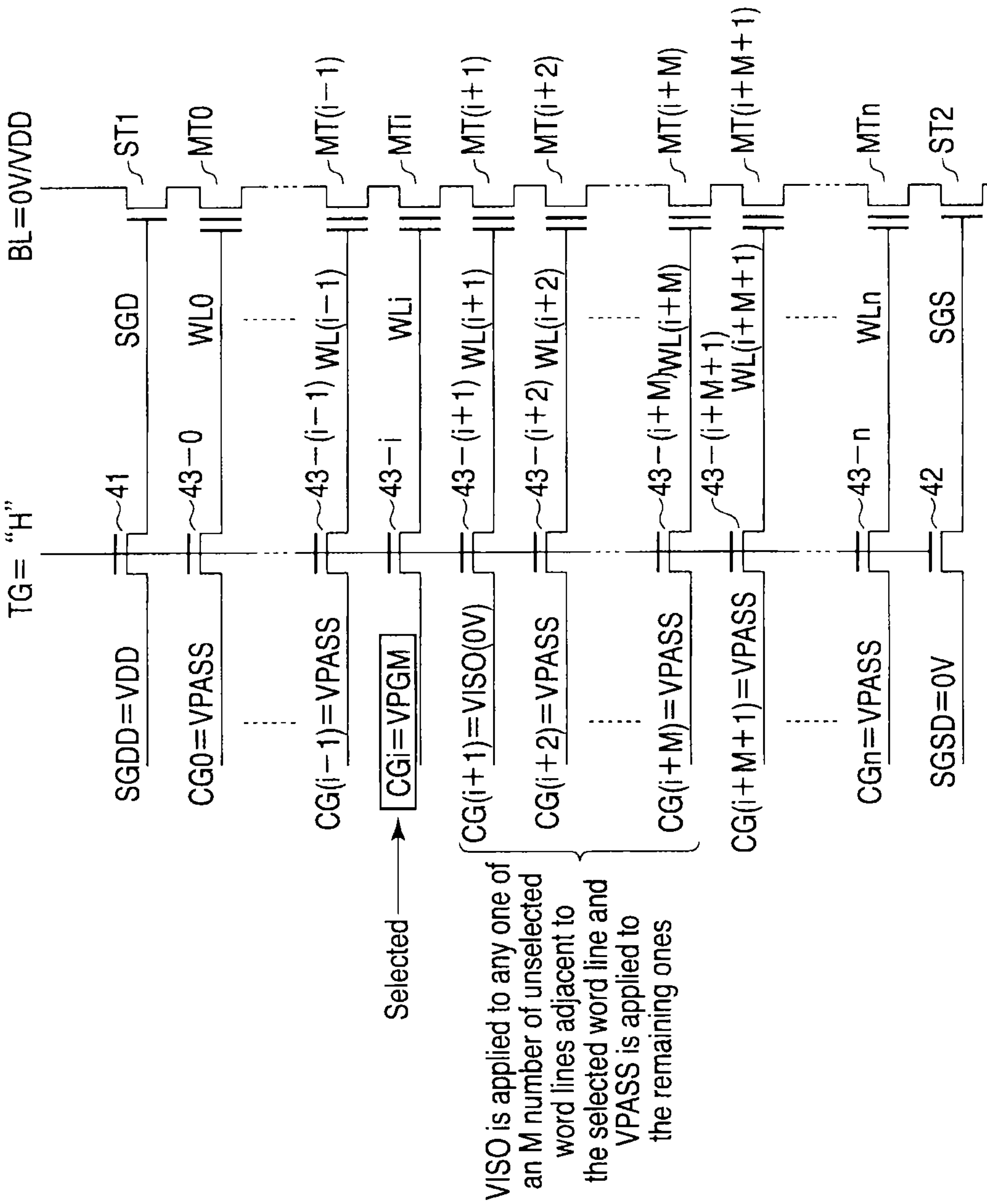
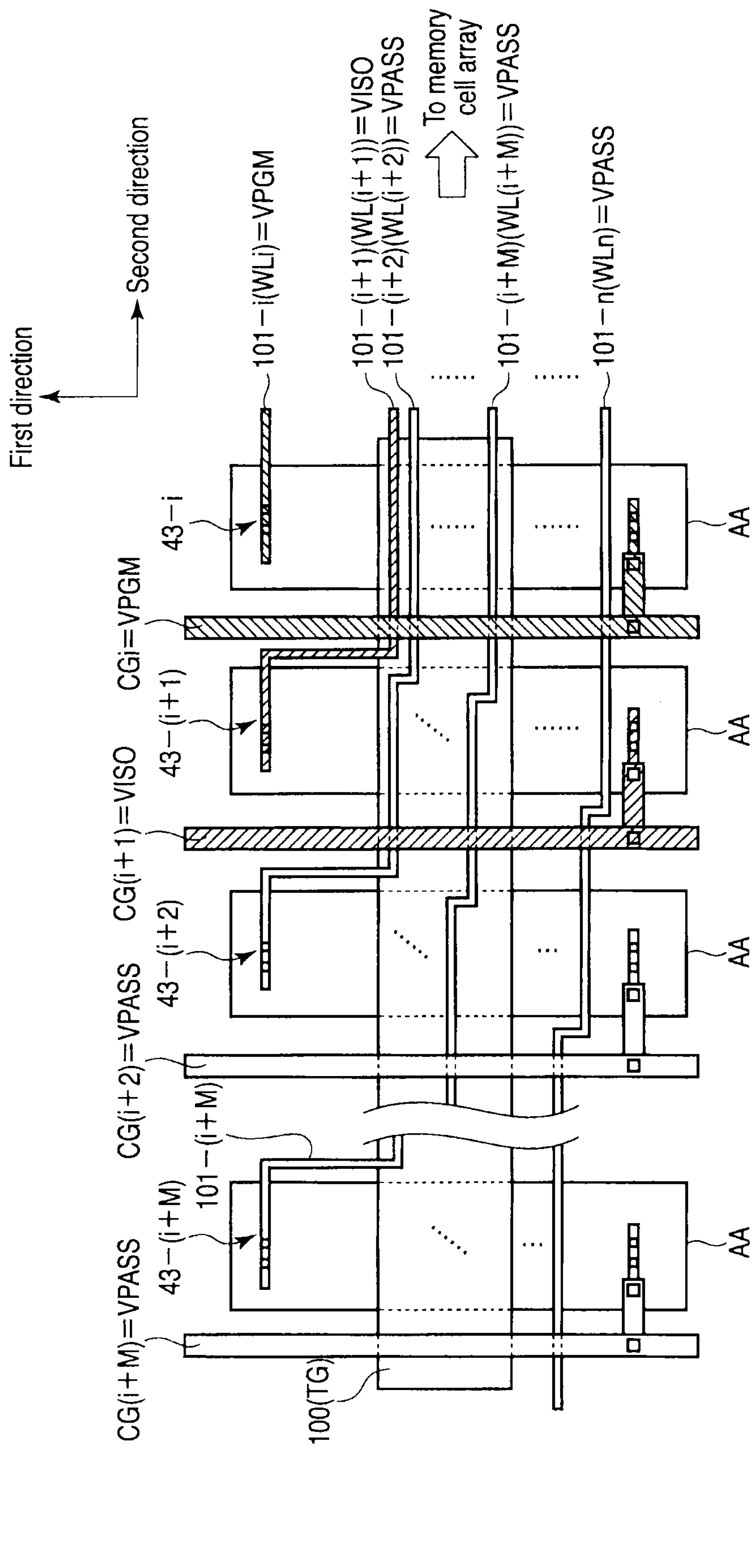

CP10
STI
101−i
114
112
101−(i+1)
111
101−(i+2)
110
AA
101−(i+M)
113
101−(i+M+1)
80
43−i
101−(i+M+2)
100(TG)
101−n
112
102
p-well
n-well
p-substrate
CP11
STI
Second direction
First direction

FIG.6


TG= "H"
BL=0V/VDD
SGDD=VDD
CG0=VPASS
CG(i−1)=VPASS
CGi=VPGM
CG(i+1)=VISO(0V)
CG(i+2)=VPASS
CG(i+M)=VPASS
CG(i+M+1)=VPASS
CGn=VPASS
SGSD=0V
41
43−0
43−(i−1)
43−i
43−(i+1)
43−(i+2)
43−(i+M)
43−(i+M+1)
43−n
42
SGD
WL0
WL(i−1)
WLi
WL(i+1)
WL(i+2)
WL(i+M)
WL(i+M+1)
WLn
SGS
ST1
MT0
MT(i−1)
MTi
MT(i+1)
MT(i+2)
MT(i+M)
MT(i+M+1)
MTn
ST2
SL
Selected
VISO is applied to any one of an M number of unselected word lines adjacent to the selected word line and VPASS is applied to the remaining ones

F I G. 7


First direction
Second direction
101−i(WLi)=VPGM
101−(i+1)(WL(i+1))=VISO
101−(i+2)(WL(i+2))=VPASS
To memory cell array
101−(i+M)(WL(i+M))=VPASS
101−n(WLn)=VPASS
43−i
CGi=VPGM
43−(i+1)
CG(i+1)=VISO
43−(i+2)
CG(i+2)=VPASS
101−(i+M)
43−(i+M)
CG(i+M)=VPASS
100(TG)
AA
AA
AA
AA

F I G. 8

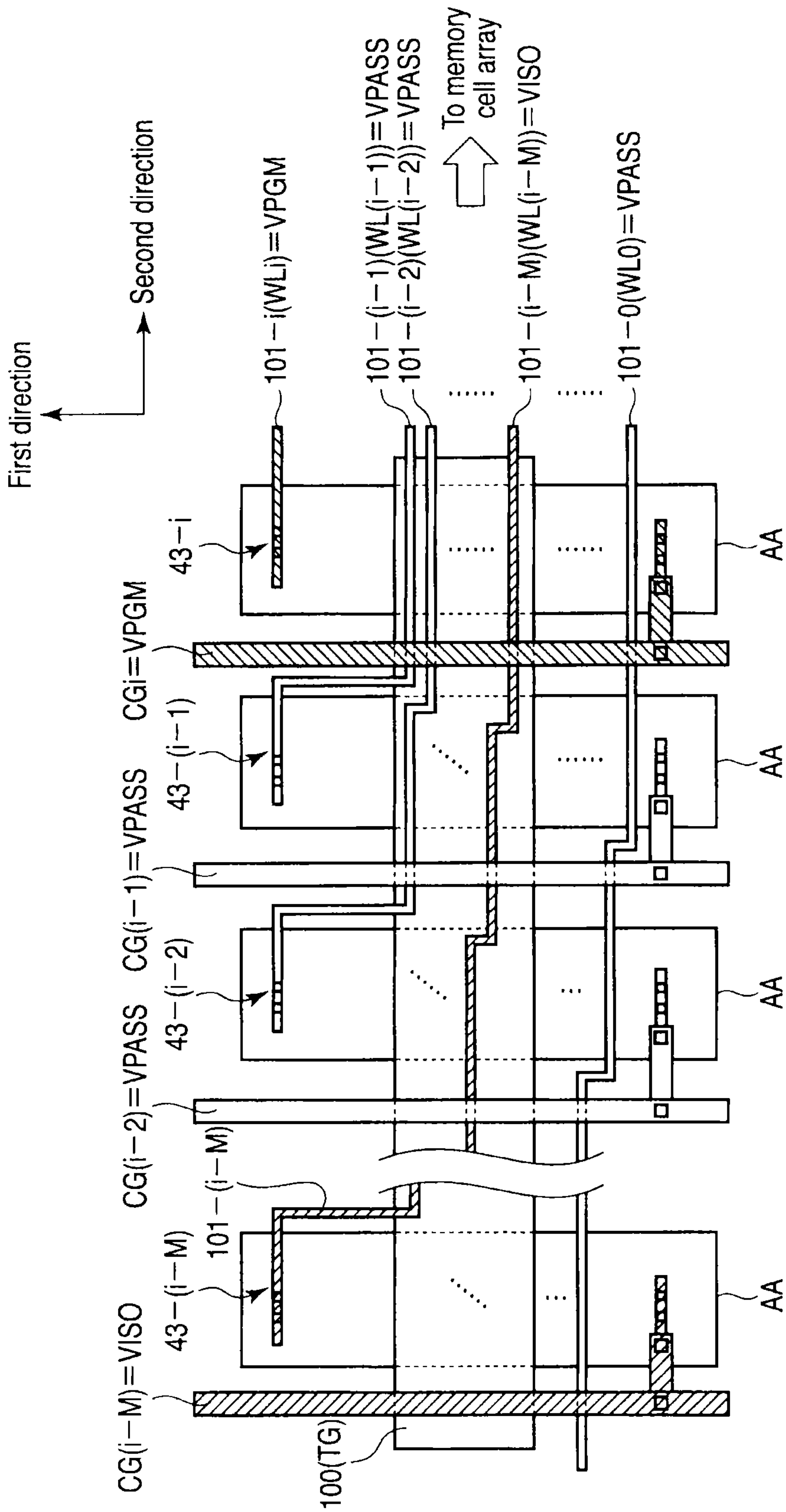
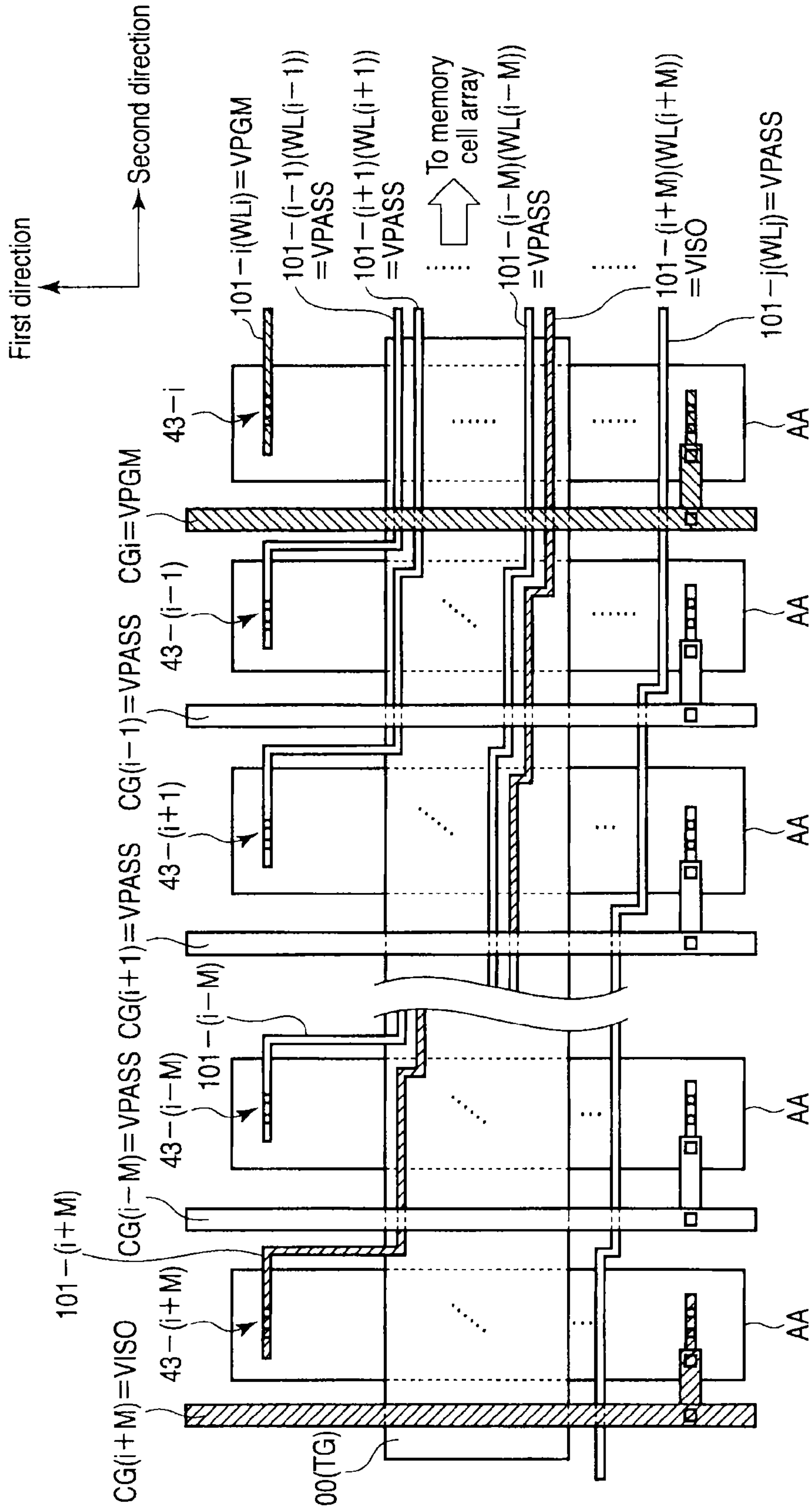

First direction
Second direction
To memory cell array
101−i(WLi)=VPGM
101−(i−1)(WL(i−1))=VPASS
101−(i−2)(WL(i−2))=VPASS
101−(i−M)(WL(i−M))=VISO
101−0(WL0)=VPASS
43−i
CGi=VPGM
43−(i−1)
CG(i−1)=VPASS
43−(i−2)
CG(i−2)=VPASS
101−(i−M)
43−(i−M)
CG(i−M)=VISO
100(TG)
AA
AA
AA
AA

FIG. 9



First direction
Second direction
101−i(WLi)=VPGM
101−(i−1)(WL(i−1))
=VPASS
101−(i+1)(WL(i+1))
=VPASS
To memory
cell array
101−(i−M)(WL(i−M))
=VPASS
101−(i+M)(WL(i+M))
=VISO
101−j(WLj)=VPASS
43−i
CGi=VPGM
43−(i−1)
CG(i−1)=VPASS
43−(i+1)
CG(i+1)=VPASS
101−(i−M)
43−(i−M)
CG(i−M)=VPASS
101−(i+M)
43−(i+M)
CG(i+M)=VISO
100(TG)
AA

F I G. 10

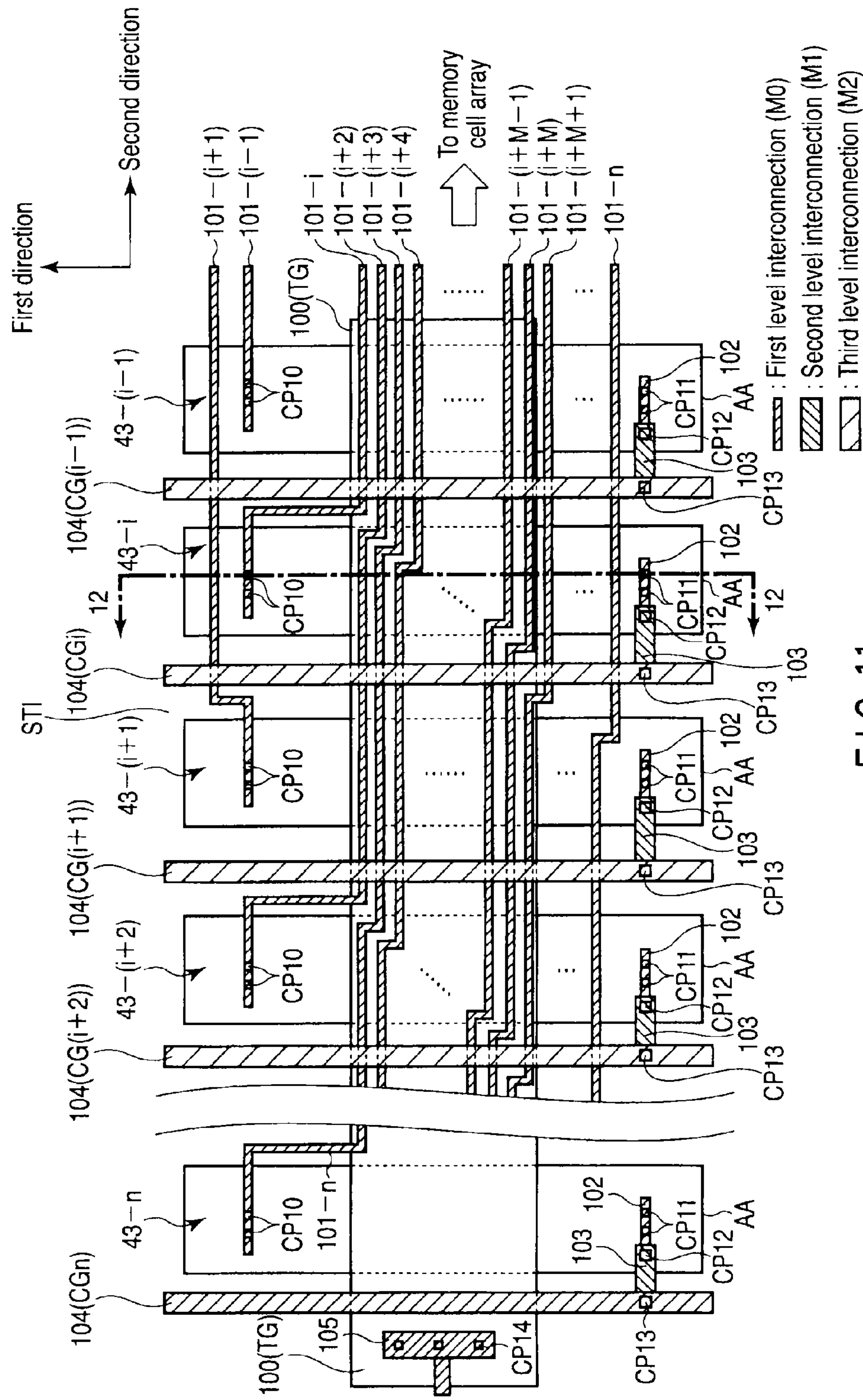
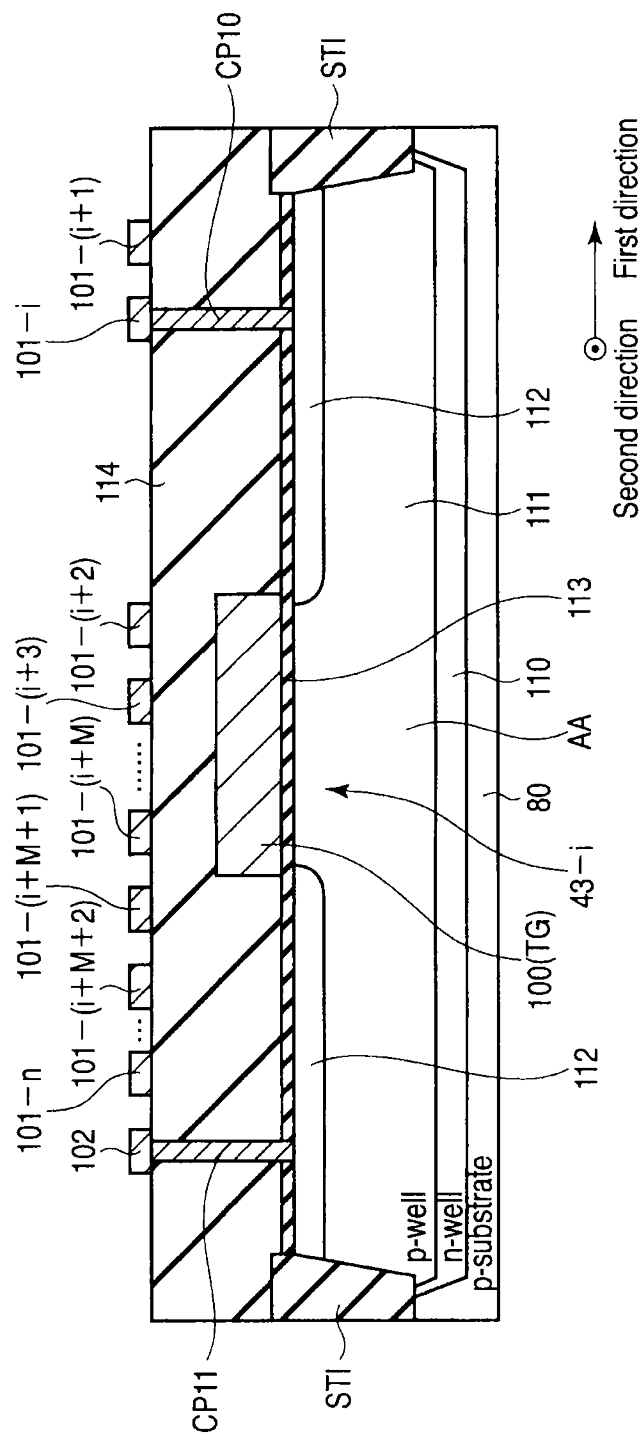
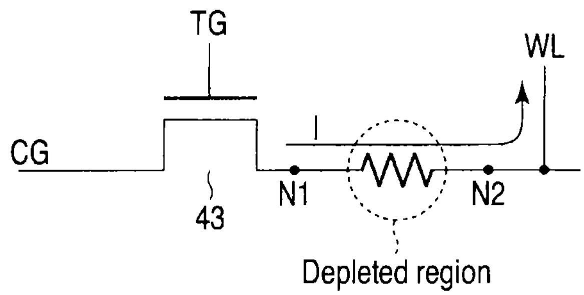

First direction
Second direction
To memory cell array
101−(i+1)
101−(i−1)
101−i
101−(i+2)
101−(i+3)
101−(i+4)
101−(i+M−1)
101−(i+M)
101−(i+M+1)
101−n
100(TG)
43−(i−1)
43−i
43−(i+1)
43−(i+2)
43−n
104(CG(i−1))
104(CGi)
104(CG(i+1))
104(CG(i+2))
104(CGn)
STI
12
CP10
CP11
CP12
CP13
CP14
102
103
105
AA
: First level interconnection (M0)
: Second level interconnection (M1)
: Third level interconnection (M2)

FIG. 11

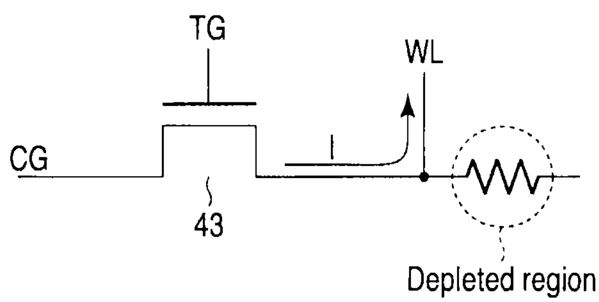

CP10
STI
101−(i+1)
101−i
114
112
111
113
101−(i+2)
101−(i+3)
101−(i+M)
101−(i+M+1)
101−(i+M+2)
101−n
102
100(TG)
AA
110
80
43−i
112
p-well
n-well
p-substrate
CP11
STI
Second direction
First direction

F I G. 12



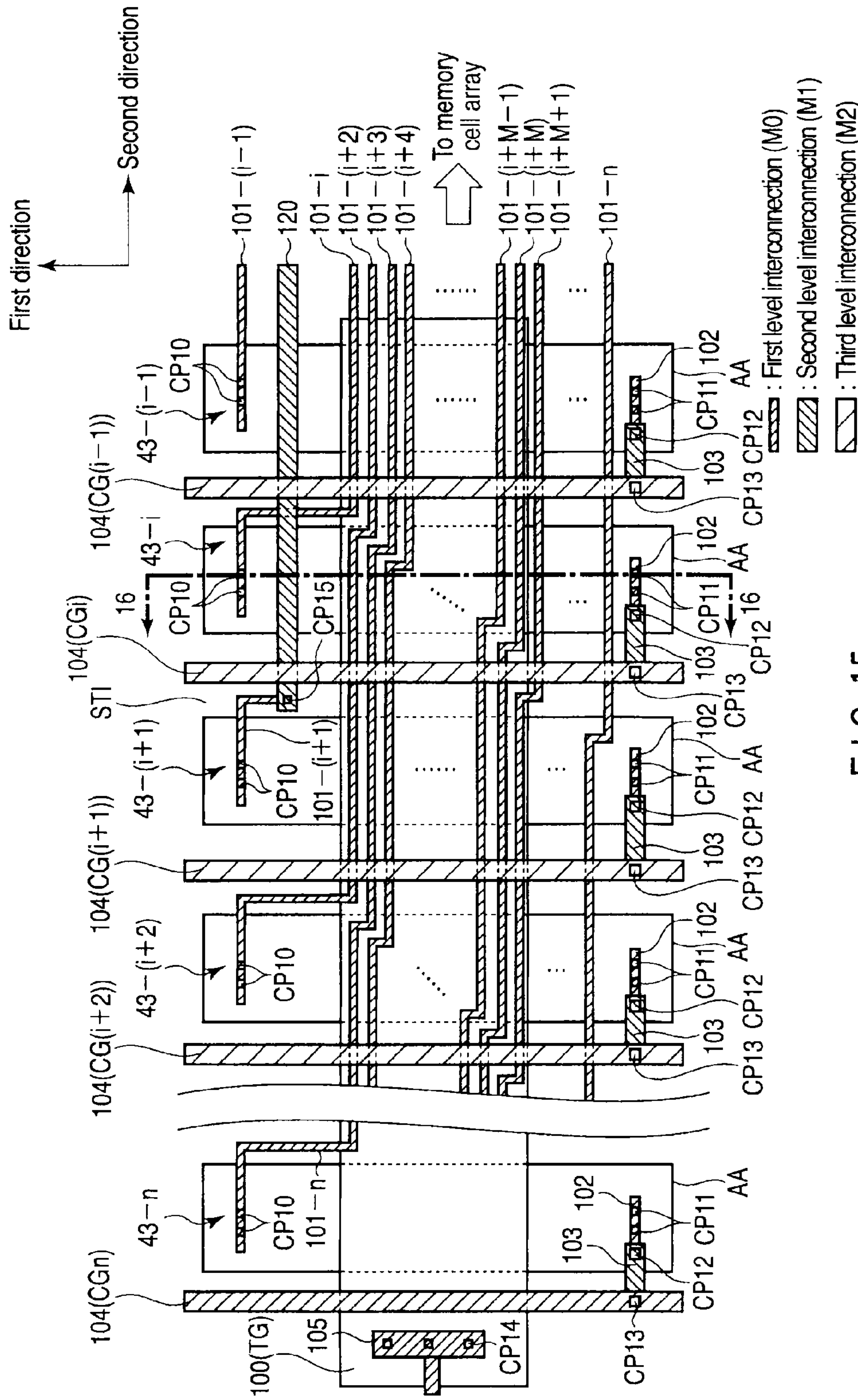
TG
WL
I
CG
N1
N2
43
Depleted region

F I G. 13

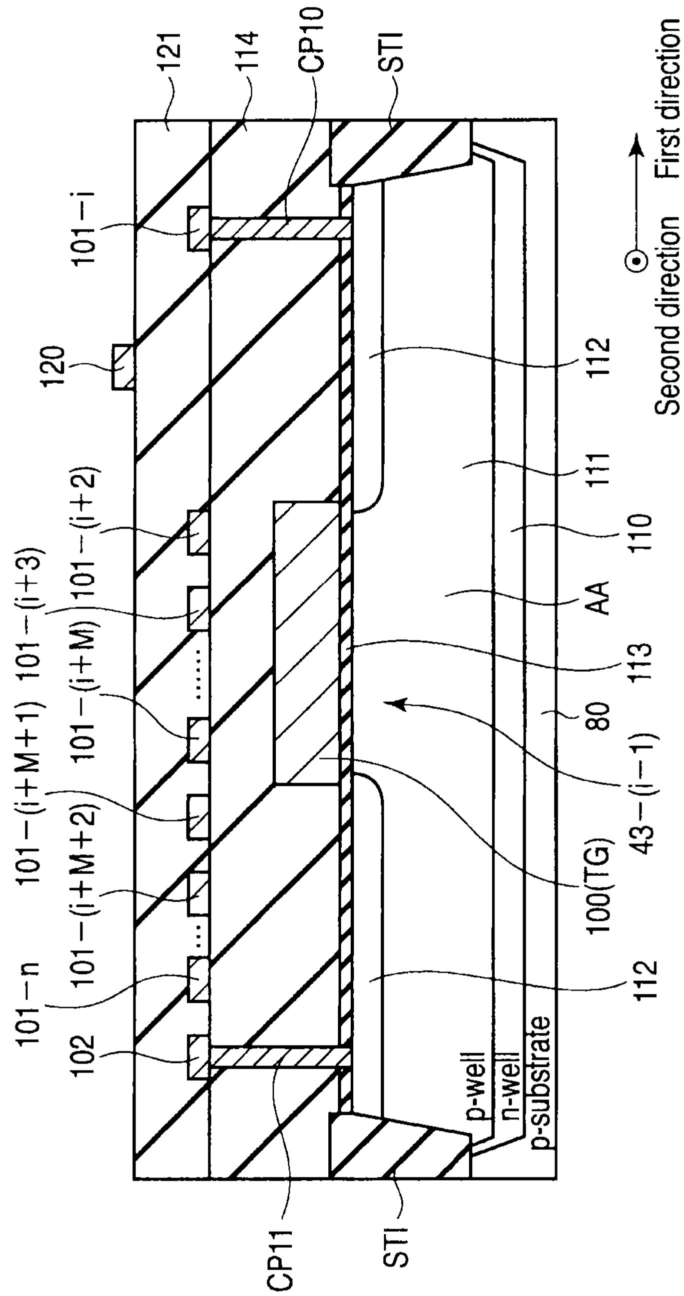


TG
WL
I
CG
43
Depleted region

F I G. 14


First direction
Second direction
To memory cell array
101−(i−1)
120
101−i
101−(i+2)
101−(i+3)
101−(i+4)
101−(i+M−1)
101−(i+M)
101−(i+M+1)
101−n
43−(i−1)
43−i
43−(i+1)
43−(i+2)
43−n
104(CG(i−1))
104(CGi)
104(CG(i+1))
104(CG(i+2))
104(CGn)
100(TG)
105
CP10
CP11
CP12
CP13
CP14
CP15
101−(i+1)
101−n
STI
16
102
103
AA
: First level interconnection (M0)
: Second level interconnection (M1)
: Third level interconnection (M2)

F I G. 15


121
114
CP10
STI
101−i
120
112
111
110
AA
113
80
43−(i−1)
100(TG)
112
101−(i+2)
101−(i+3)
101−(i+M)
101−(i+M+1)
101−(i+M+2)
101−n
102
CP11
STI
p-well
n-well
p-substrate
Second direction
First direction

F I G. 16

SEMICONDUCTOR MEMORY DEVICE WITH MEMORY CELLS EACH INCLUDING A CHARGE ACCUMULATION LAYER AND A CONTROL GATE

CROSS-REFERENCE TO RELATED APPLICATIONS

This present application is a continuation of U.S. application Ser. No. 12/695,623, filed Jan. 28, 2010, which claims the benefit of priority from prior Japanese Patent Application No. 2009-019678, filed Jan. 30, 2009. The entire contents of the above-applications are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a semiconductor memory device. More particularly, this invention relates to a semiconductor memory device with memory cells each including a charge accumulation layer and a control gate.

2. Description of the Related Art

An electrically erasable and programmable ROM (EEPROM) has been known as a nonvolatile semiconductor memory capable of rewriting data electrically. In addition, a NAND flash memory has been known as an EEPROM capable of high capacity and high integration.

In a NAND flash memory, it is necessary to apply a high voltage to a word line to write or erase data. Therefore, the NAND flash memory is provided with a row decoder including a transfer transistor for transferring a high voltage to the word line. Such a configuration has been disclosed in Jpn. Pat. Appln. KOKAI Publication No. 2002-63795.

BRIEF SUMMARY OF THE INVENTION

A semiconductor memory device according to an aspect of the present invention includes:

a memory cell unit in which an (N+1) number of memory cells (N is a natural number not less than 1), including charge accumulation layers and control gates formed on the charge accumulation layers, are connected in series;

an (N+1) number of word lines connected to the control gates of 0-th to N-th memory cells connected in series in a one-to-one correspondence;

a driver circuit which supplies a voltage to the memory cells; and

an (N+1) number of first transistors which are formed on (N+1) number of element regions provided in a semiconductor substrate, include gate electrodes formed above the element regions with gate insulating films interposed therebetween, and transfer the voltage to the word lines respectively, each of the first transistors including two impurity diffused layers which are formed at the surface of one of the element regions and one of which is connected to the driver circuit and the other of which is connected to one of the word lines,

wherein the (N+1) number of element regions are electrically separated from one another and the gate electrodes are connected in common, and

above one of the first transistors which transfers the voltage to an i-th (i is a natural number in the range of 0 to N) word line, M (M<N) of the word lines close to the i-th word line pass through a region above the gate electrode by a first level interconnection without passing over the impurity diffused layers.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

FIG. **1** is a block diagram of a flash memory according to a first embodiment of the invention;

FIG. **2** is a plan view of a memory cell array according to the first embodiment;

FIGS. **3** and **4** are sectional views taken along line **3-3** and line **4-4** of FIG. **2**, respectively;

FIG. **5** is a plan view of a row decoder according to the first embodiment;

FIG. **6** is a sectional view taken along line **6-6** of FIG. **5**;

FIG. **7** is a circuit diagram of a memory cell unit and a row decoder according to the first embodiment;

FIG. **8** is a plan view of a row decoder according to the first embodiment;

FIGS. **9** and **10** are plan views of a row decoder according to a first and a second modification of the first embodiment, respectively;

FIG. **11** is a plan view of a row decoder according to a second embodiment of the invention;

FIG. **12** is a plan view taken along line **12-12** of FIG. **11**;

FIG. **13** is an equivalent circuit diagram of a MOS transistor;

FIG. **14** is an equivalent circuit diagram of a MOS transistor according to the second embodiment;

FIG. **15** is a plan view of a row decoder according to a third embodiment of the invention; and

FIG. **16** is a plan view taken along line **16-16** of FIG. **15**.

DETAILED DESCRIPTION OF THE INVENTION

First Embodiment

A semiconductor memory device according to a first embodiment of the invention will be explained. FIG. **1** is a block diagram of a NAND flash memory according to the first embodiment.

<Overall Configuration of NAND Flash Memory>

As shown in FIG. **1**, the NAND flash memory **1** includes a memory cell array **10**, a sense amplifier **20**, a source line driver **30**, a row decoder **40**, a driver circuit **50**, a voltage generator circuit **60**, and a control circuit **70**.

The memory cell array **10** includes a plurality of memory cell units **11**. Each of the memory cell units **11** includes an (n+1) number of memory cell transistors MT**0** to MTn ((n+1) is a natural number not less than 2) and select transistors ST**1**, ST**2**. When there is no need to distinguish between memory cell transistors MT**0** to MTn, they will simply be referred to as memory cell transistors MT. The number of memory cell transistors MT is, for example, 8, 16, 32, 64, 128, or 256, and is nonlimiting. Each of memory cell transistors MT has a stacked gate structure including a charge accumulation layer (e.g., a floating gate), formed on a semiconductor device with a gate insulating film interposed therebetween, and a control gate, formed on the charge accumulation layer with an inter-gate insulating film interposed therebetween. Adjacent memory cell transistors MT share a source and a drain. The memory cell transistors MT are arranged between select transistors ST**1**, ST**2** in such a manner that their current paths are connected in series. The drain region on one end side (memory cell transistor MT**0**) of the memory cell transistors MTs connected in series is connected to the source of select transistor ST**1** and the source region on the other end side (memory cell transistor MTn) is connected to the drain of select transistor ST**2**.

The control gates of memory cell transistors MT0 to MTn in the same row are connected to any one of word lines WL0 to WLn in a common connection manner. The gates of select transistors ST1 of the memory cells in the same row are connected to a select gate line SGD in a common connection manner. The gates of select transistors ST2 of the memory cells in the same row are connected to a select gate line SGS in a common connection manner. To simplify the explanation, word lines WL0 to WLn will sometimes simply be referred to as word lines WL.

A plurality of memory cell units **11** connected to the same word line WL and select gate lines SGD, SGS form a memory block. Data is erased in memory blocks simultaneously. In addition, data is written simultaneously into a plurality of memory cell transistors MT connected to the same word line WL. This writing unit is called a page.

Although not shown in FIG. **1**, a plurality of memory blocks is arranged in a direction perpendicular to the word line WL. The drains of select transistors ST**1** in the same column are connected to any one of bit lines BL to BLm (m is a natural number) in a common connection manner. Bit lines BL**0** to BLm will sometimes simply be referred to as bit lines BL. The sources of select transistors ST**2** are connected to a source line SL in a common connection manner. Both of the select transistors ST**1**, ST**2** are not necessarily needed. Only one of the select transistors ST**1**, ST**2** may be used, provided that the memory cell unit **11** can be selected.

Sense amplifier **20**, in a read operation, senses data read from a memory cell transistor MT onto a bit line BL and amplifies the data. In a write operation, sense amplifier **20** transfers write data to a bit line BL. More specifically, sense amplifier **20** applies a voltage corresponding to write data to a bit line BL.

Source line driver **30** applies a voltage to the source line SL.

Row decoder **40** includes MOS transistors **41**, **42** provided for select gate lines SGD, SGS respectively, MOS transistors **43-0** to **43**-*n* provided for word lines WL**0** to WLn respectively, and a block decoder **44**.

One end of the current path of MOS transistor **41** is connected to select gate line SGD. One end of the current path of MOS transistor **42** is connected to select gate line SGS. The other ends of MOS transistors **41**, **42** are connected to signal lines SGDD, SGSD, respectively.

One end of each of MOS transistors **43-0** to **43**-*n* is connected to the corresponding one of word lines WL**0** to WLn. The other end of each of MOS transistors **43-0** to **43**-*n* is connected to the corresponding one of signal lines CG**0** to CGn. That is, MOS transistors **41**, **42** function as transfer transistors that transfer the potentials on signal lines SGDD, SGSD to select gate lines SGD, SGS, respectively. MOS transistors **43-0** to **43**-*n* function as transfer transistors that transfer the potentials on signal lines CG**0** to CGn to word lines WL**0** to WLn, respectively. Hereinafter, when there is no need to distinguish between MOS transistors **43-0** to **43**-*n*, they will simply be referred to as MOS transistors **43**. In addition, when there is no need to distinguish between signal lines CG**0** to CGn, they will simply be referred to as signal lines CG. The gates of MOS transistors **41** to **43** connected not only to select gate lines SGD, SGS connected to select transistors ST**1**, ST**2** and memory cell transistors MT but also to word lines WL in the same memory block are connected to the same signal line TG.

Block decoder **44** externally receives a block address and decodes the block address. Then, block decoder **44** selects signal line TG to which MOS transistor **43** corresponding to memory cell unit **11** that includes a selected memory cell transistor to be written into, read from, or erased from is connected, thereby turning on MOS transistors **41** to **43**.

Driver circuit **50** supplies a voltage necessary to write, read, or erase data to signal line SGDD, SGSD, and CG according to the result of decoding the page address. Those voltages are generated by the voltage generator circuit **60**. The voltages applied to signal lines SGDD, SGSD, and CG will be described in detail later.

Control circuit **70** externally receives a command and controls the operation of the voltage generator circuit **60** according to the command. That is, in a write, read, or erase operation, or the like, control circuit **70** instructs voltage generator circuit **60** to generate a suitable voltage.

Voltage generator circuit **60** includes a charge pump circuit. According to the instruction given by control circuit **70**, voltage generator circuit **60** generates a voltage necessary to write, read, or erase data and supplies the generated voltage to driver circuit **50**.

<Configuration of Memory Cell Array **10**>

Next, the configuration of memory cell array **10** will be explained in detail.

<Planar Configuration>

First, a planar configuration of memory cell array **10** will be explained with reference to FIG. **2**. FIG. **2** is a plan view of memory cell array **10**.

As shown in FIG. **2**, in a semiconductor substrate **80**, a plurality of strips of element regions AA extending in a first direction is also provided in a second direction, perpendicular to the first direction. An element isolating region STI is formed between adjacent element regions AA. The element isolating regions STI electrically separate the element regions AA from one another. On the semiconductor substrate **80**, the strips of word lines WL and select gate lines SGD, SGS extending in the second direction are formed so as to cross a plurality of element regions AA. Floating gates FG are provided in the regions where word lines WL cross element regions AA. Although the width of floating gate FG is narrower than that of element region AA in FIG. **2**, the width of floating gate FG may be equal to or greater than the width of element region AA. Memory cell transistors MT are provided in the regions where word lines WL cross element regions AA. In the region where select gate lines SGD cross element regions AA, select transistors ST**1** are provided. In the region where select gate lines SGS cross element regions AA, select transistors ST**2** are provided. In element regions AA between adjacent word lines WL, between adjacent select gate lines, and between a word line and a select gate line adjacent in the first direction, impurity diffused layers serving as the source regions or drain regions of memory cell transistors MT and select transistors ST**1**, ST**2** are formed.

An impurity diffused layer formed in element region AA between adjacent select gate lines SGD in the first direction functions as the drain region of select transistor ST**1**. On the drain region, a contact plug CP**1** is formed. Contact plug CP**1** is connected to a bit line BL strip extending in the first direction. An impurity diffused layer formed in element region AA between adjacent select gate lines SGS in the first direction functions as the source region of select transistor ST**2**. On the source region, a contact plug CP**2** is formed. Contact plug CP**2** is connected to a source line (not shown).

<Cross-Section Configuration>

Next, a cross-section configuration of memory cell unit **11** will be explained with reference to FIGS. **3** and **4**. FIG. **3** is a sectional view taken along line **3-3** of FIG. **2**. FIG. **4** is a sectional view taken along line **4-4** of FIG. **2**.

As shown in FIGS. **3** and **4**, an n-well region **81** is formed at the surface of a p-type semiconductor substrate **80** and a p-well region **82** is formed at the surface of the n-well region **81**. At the surface of the p-well region **82**, a plurality of strips of element isolating regions STI extending in the first direction are also formed in the second direction. As a result, a strip of element regions AA extending in the first direction is formed, being surrounded by element isolating regions STI.

On the element isolating region AA, a gate insulating film **83** is formed. On the gate insulating film **83**, the gate electrodes of the memory cell transistors MT and select transistors ST**1**, ST**2** are formed. Each of the gate electrodes of the memory cell transistors MT and select transistors ST**1**, ST**2** includes a polysilicon layer **84** formed on the gate insulating film **83**, an inter-gate insulating film **85** formed on the polysilicon layer **84**, and a polysilicon layer **86** formed on the inter-gate insulating film **85**. The inter-gate insulating film **85** is formed by using of, for example, a silicon dioxide film, or an ON, an NO, or an ONO film which have a stacked structure of a silicon dioxide film and a silicon nitride film, or a stacked structure including those, or a stacked structure of a TiO_2, HfO_2, Al_2O_3, HfAlOx, or HfAlSi film and a silicon dioxide or a silicon nitride film.

In the memory cell transistors MT, the polysilicon layers **84** function as floating gates (FG). The polysilicon layers **86** adjacent in the second direction are connected to each other and function as a control gate (word line WL). In the select transistors ST**1**, ST**2**, the polysilicon layers **84**, **86** adjacent in the second direction are connected to each other. The polysilicon layers **84**, **86** function as select gate lines SGS, SGD. Only the polysilicon layers **84** may function as select gate lines. In this case, the polysilicon layers **86** of the select transistors ST**1**, ST**2** are set at a specific potential or in a floating state. At the surface of the semiconductor substrate **80** between gate electrodes, an n^+-type impurity diffused layer **87** is formed. The impurity diffused layer **87**, which is shared by adjacent transistors, functions as a source (S) or a drain (D). The region between a source and a drain adjacent to each other functions as a channel region serving as an electron moving region. These gate electrodes, impurity diffused layers **87**, and channel regions form MOS transistors which function as memory cell transistors MT and select transistors ST**1**, ST**2**.

On the semiconductor substrate **80**, an interlayer insulating film **88** is formed so as to cover the memory cell transistors MT and select transistors ST**1**, ST**2**. In the interlayer insulating film **88**, a contact plug CP**2** reaching the impurity diffused layer (source S) **87** of select transistor ST**2** on the source side is formed. On the interlayer insulating film **88**, a metal wiring layer **89** connected to the contact plug CP**2** is formed. The metal wiring layer **89** functions as a source line SL. Further, in the interlayer insulating film **88**, a contact plug CP**3** reaching the impurity diffused layer (drain D) **87** of select transistor ST**1** on the drain side is formed. On the interlayer insulating film **88**, a metal wiring layer **90** connected to the contact plug CP**3** is formed.

On the interlayer insulating film **88**, an interlayer insulating film **91** is formed so as to cover the metal wiring layers **89**, **90**. In the interlayer insulating film **91**, a contact plug CP**4** reaching the metal wiring layer **90** is formed. On the interlayer insulating film **91**, a metal wiring layer **92** connected to a plurality of contact plugs CP**4** in common is formed. The metal wiring layer **92** functions as a bit line BL. The contact plugs CP**3**, CP**4**, and metal wiring layer **90** correspond to the contact plugs CP**1** of FIG. **2**.

<Detailed Configuration of Row Decoder **40**>

Next, a detailed configuration of the row decoder **40** will be explained, particularly focusing on MOS transistor **43**.

<Planar Configuration>

First, a planar configuration will be explained with reference to FIG. **5**. FIG. **5** is a plan view of a region where MOS transistors **43** are formed in the row decoder **40**.

As shown in FIG. **5**, an (n+1) number of strips of element regions AA extending in the first direction are also provided in the second direction in the semiconductor substrate **80**. Between element regions AA, element isolating regions STI are formed. The element regions AA are electrically separated by the element isolating regions STI. On each of the element regions AA, a MOS transistor **43** is formed.

Specifically, on each of the element regions AA, the gate electrode **100** of a MOS transistor **43** is formed so as to cross the individual element regions AA in the second direction. Further, in each of the element regions AA, impurity diffused layers serving as one and the other ends of the current path of the MOS transistor **43** are formed. Here, i in FIG. **5** is in the range of 0 to n. MOS transistors **43-0** to **43-*n*** connected to the same memory block are arranged in a line in the second direction. The gate electrodes **100** of these MOS transistors are connected in common and function as a signal line TG. Accordingly, the gate electrodes **100** form strips extending in the second direction. In the example of FIG. **5**, MOS transistors **43-0** to **43-*n*** are arranged, starting with the one closest to the memory cell array **10**. That is, MOS transistor **43-0** is provided closest to the memory cell array **10** and MOS transistor **43-*n*** is provided farthest away from the memory cell array **10**.

On one end of the current path of MOS transistor **34**, a contact plug CP**10** is formed. One end of the current path of MOS transistor **34** is connected via contact plug CP**10** to a metal wiring layer (M**0**) **101** in a first level layer. The metal wiring layer (M**0**: first level interconnection) is a metal wiring layer in the lowest layer of the NAND flash memory **1**. The metal wiring layer **101** is drawn to the boundary between the row decoder **40** and memory cell array **10** and connected to a word line WL. When it is necessary to distinguish between the metal wiring layers **101** connected to MOS transistors **43-0** to **43-*n***, they will be referred to as metal wiring layers **101-0** to **101-*n***. That is, metal wiring layers **101-0** to **101-*n*** are connected to word lines WL**0** to WLn, respectively. In other words, it may be said that metal wiring layers **101-0** to **101-*n*** function as part of word lines WL**0** to WLn.

The other end of the current path of MOS transistor **34** is connected to a metal wiring layer **102** in the first level layer via a contact plug CP**11**. The metal wiring layer **102** is connected to a metal wiring layer (M**1**: second level interconnection) **103** in a second level layer higher than the metal wiring layer (M**0**) via a contact plug CP**12**. The metal wiring layer **103** is connected to a metal wiring layer (M**2**: third level interconnection) **104** in a third level layer higher than the metal wiring layer in the second level layer via a contact plug CP**13**. The metal wiring layer **104**, which functions as a signal line CG, has the form of a strip and extends in the first direction and passes through a region between adjacent element regions AA. The gate electrode **100** is connected to a metal wiring layer **105** in the first level layer with a contact plug CP**14** and is connected to a block decoder **44** with the metal wiring layer **105**.

In the first embodiment, a MOS transistor **43** connected to a word line WL closer to select gate line SGD is arranged closer to the memory cell array **10** in the row decoder **40**. Accordingly, metal wiring layers **101**-(*i*+1) to **101-*n*** connected to MOS transistors **43**-(*i*+1) to **43-*n*** that transfer voltages to word lines WL(i+1) to WLn pass over MOS transistors **43-0** to **43-*i*** that transfer voltages to word line WLi and word lines WL**0** to WL(i−1). The word lines WL(i+1) to WLn is closer to select gate line SGS than a certain word line WLi is. The word line WL0 to WL (i−1) is closer to select gate line SGD than word line WLi is.

In this case, of metal wiring layers **101**-(*i*+1) to **101**-*n*, metal wiring layers **101**-(*i*+1) to **101**-(*i*+M) connected to an M number of word lines WL(i+1) to WL(i+M) (M is a natural number not less than 1) adjacent to word line WLi pass over the gate electrode **100** on an element region AA where MOS transistor **43**-*i* has been formed. Metal wiring layers **101**-(*i*+M+1) to **101**-*n* connected to the remaining word lines WL(i+M+1) to WLn pass over a region between contact plug CP**11** (or CP**10**) and gate electrode **100**.

Accordingly, as shown in FIG. **5**, metal wiring layers **101** passing over the gate electrode **100** of each MOS transistor **43** is shifted at the position corresponding to each MOS transistor **43**.

<Sectional Configuration>

Next, a sectional configuration of a MOS transistor **43** in the row decoder **40** will be explained with reference to FIG. **6**. FIG. **6** is a sectional view taken along line **6**-**6** of FIG. **5**.

As shown in FIG. **6**, element isolating regions STI are formed in the surface of the p-type semiconductor substrate **80**, thereby forming an element region AA surrounded by the element isolating regions STI. At the surface of the element region AA, an n-well region **110** is formed. In the surface region of n-well region **110**, a p-well region **111** is formed. In the surface region of p-well region **111**, two separate impurity diffused layers **112** are formed. The impurity diffused layers **112** function as the source or drain of MOS transistor **43**.

Above p-well region ill between impurity diffused layers **112**, a gate electrode **100** of MOS transistor **43** is formed with a gate insulating film **113** interposed therebetween. Gate electrode **100** is formed of, for example, a polysilicon layer. The sectional configuration of gate electrode **100** has the same stacked structure as that of the gate electrode of each of select transistors ST**1**, ST**2**. The gate insulating film **113** is larger than the gate insulating film **83**, which enables MOS transistor **43** to withstand a higher voltage than the memory cell transistors MT and select transistors ST**1**, ST**2**.

On the semiconductor substrate **80**, an interlayer insulating film **114** is formed so as to cover MOS transistor **43** configured as described above. In the interlayer insulating film **114**, a contact plug CP**10** reaching one of the impurity diffused layers **112** and a contact plug CP**11** reaching the other of the impurity diffused layers **112** are formed. On the interlayer insulating film **114**, metal wiring layers **101**-*i* and **102**, respectively in contact with contact plugs CP**10** and CP**11**, are formed.

Further, on the interlayer insulating film **114**, metal wiring layers **101**-(*i*+1) to **101**-*n* are formed so as to be sandwiched between metal wiring layers **101**-*i* and **102**. Of them, metal wiring layers **101**-(*i*+1) to **101**-(*i*+M) are arranged in a region directly above gate electrode **100**. The remaining metal wiring layers **101**-(*i*+M+1) to **101**-*n* are arranged in a region directly above the impurity diffused layer **112** in contact with contact plug CP**11**.

<Write Operation of NAND Flash Memory>

Next, a write operation of the NAND flash memory **1** configured as described above will be explained. Hereinafter, a case where charges are injected into charge accumulation layer **84** to raise the threshold voltage of the memory cell transistor MT is called a "0" program. In contrast, a case where no charge is injected into charge accumulation layer **84** to prevent the threshold voltage from changing (in other words, a case where the injection of charges is suppressed to a degree that the held data does not transit to another level) is called a "1" program. FIG. **7** is a circuit diagram of memory cell unit **11** and row decoder **40** in a write operation.

When data is written, voltage generator circuit **60** generates a high positive voltage VPGM and an intermediate voltage VPASS (<VPGM) under the control of control circuit **70**. Voltage VPGM is a high voltage for injecting electrons into a charge accumulation layer by FN tunneling. Voltage VPASS is a voltage for turning on a memory cell transistor MT, regardless of held data.

Block decoder **44** decodes a block address and applies a "H"-level signal to the signal lines TG of MOS transistors **41** to **43** connected to the memory block including a memory cell transistor MT into which data is to be written (referred to as a selected cell). As a result, MOS transistors **41** to **43** turn on.

Furthermore, driver circuit **50** decodes a page address, selects signal line CGi, and applies voltage VPGM to signal line CGi. In addition, driver circuit **50** applies voltage VPASS to signal lines CG**0** to CG(i−1) closer to select gate line SGD than signal line CGi. Moreover, driver circuit **50** applies voltage VISO to any one of an M number of signal lines CG(i+1) to CG(i+M) adjacent to signal line CGi and voltage VPASS to the rest. Driver circuit **50** further applies voltage VPASS to the remaining signal lines CG(i+M+1) to CGn. Voltage VISO is a voltage for turning off a memory cell transistor MT, regardless of held data. Voltage VISO is, for example, 0 V. Hereinafter, a case where voltage VISO is applied to signal line CG(i+1) will be explained as an example.

Driver circuit **50** further applies voltage VDD and 0 V to signal lines SGDD and SGSD, respectively. Voltage VDD is a voltage for causing select transistor ST**1** to transfer "0" program data or preventing select transistor ST**1** from transferring "1" program data. In other words, voltage VDD is a voltage that turns on select transistor ST**1** at the time of the "0" program and turns it off at the time of the "1" program.

As a result, MOS transistors **41** and **42** transfer VDD and 0 V to select gate lines SGD and SGS, respectively. MOS transistor **43**-*i* transfers voltage VPGM to word line WLi (selected word line). MOS transistor **43**-(*i*+1) transfers voltage VISO to word line WL(i+1) (unselected word line). Moreover, MOS transistors **43**-**0** to **43**-(*i*−1), **43**-(*i*+2) to **43**-*n* transfer voltage VPASS to word lines WL**0** to WL(i−1), WL(i+2) to WLn (unselected word lines).

As described above, transferring the voltages to the word lines WL causes MOS transistors MT**0** to MTi, MT(i+2) to MTn to turn on, forming a channel. In contrast, memory cell transistor MT(i+1) goes off, forming no channel. That is, the channels of memory cell transistors MT**0** to MTi are conducting and the channels of memory cell transistors MT(i+2) to MTn are conducting. However, MOS transistors MT**0** to MTi and memory cell transistors MT(i+2) to MTn are separated by memory cell transistor MT(i+1). Since 0 V is applied to select gate line SGS, select transistor ST**2** is off. In contrast, select transistor ST**1** turns on or off, depending on program data.

When the "0" program is executed, sense amplifier **20** applies a write voltage (e.g., 0 V) to a bit line BL. Accordingly, select transistor ST**1** turns on, transferring 0 V applied to the bit line to the channels of memory cell transistors MT**0** to MTi. Then, in the memory cell transistor MTi connected to the selected word line WLi, the potential difference between the gate and channel is almost VPGM, with the result that charges are injected into charge accumulation layer **84**. As a result, the threshold voltage of memory cell transistor MTi rises, causing the "0" program to be executed.

When the "1" program is executed, sense amplifier **20** applies a write inhibit voltage (e.g., VDD) to a bit line, turning off select transistor ST**1**. Accordingly, the channels of memory cell transistors MT**0** to MTi in the memory cell unit

11 go into an electrically floating state. Then, the potentials at the channels of memory cell transistors MT**0** to MTi rise as a result of coupling with the gate potentials (VPGM, VPASS). Therefore, in memory cell transistor MTi connected to the selected word line WLi, the potential difference between the gate and channel is insufficient, preventing charges from being injected into charge accumulation layer **84** (to a degree that the held data transits). As a result, the threshold voltage of memory cell transistor MTi remains unchanged, causing the "1" program to be executed.

<Effect>

As described above, the semiconductor memory device of the first embodiment can suppress a decrease in the voltage transfer capability of MOS transistor **43** and improve the operation reliability of the NAND flash memory **1**. This effect will be explained below.

(1) Local Self-Boost

In the field of NAND flash memories, a method of writing data by a self-boost method has been known. The self-boost method is the technique for turning off select transistors ST**1**, ST**2** of memory cell unit **11** including the MOS transistors MT that run the "1" program, thereby bringing the channels of the memory cell transistors MT included in the memory cell unit **11** into an electrically floating state, which raises the potentials at the channels by coupling with the word lines WL. As a result, in memory cell transistor MTi connected to the selected word line WLi, the potential difference between the gate and channel decreases, preventing charges from being injected into the charge accumulation layer, which causes the "1" program to be executed.

In the self-boost method, it is important to boost the channel potential efficiently. The reason for this is that, if the boost is insufficient, there is a possibility that the "0" program will be erroneously executed to the MOS transistors MT to which the "1" program is supposed to be executed. If self-boost is performed using data-written MOS transistors MT, the boost efficiency might decrease, depending on the data held in the MOS transistors MT.

As explained in FIG. **7**, voltage VISO is applied to at least one of the unselected word lines (e.g., word line WL(i+1)). This unselected word line is closer to source line SL than the selected word line WLi is. The voltage VISO causes memory cell transistor MT(i+1) to go off. This prevents programmed memory cell transistors MT(i+2) to MTn closer to the source than memory cell transistor MT(i+1) from contributing to self-boost. Accordingly, the boost efficiency of the channels of memory cell transistors MT**0** to MTi can be increased. This method is known as local self-boost.

(2) Miniaturization

In recent years, NAND flash memories have been miniaturized more and more and the size of one memory block has been reduced further. As a result, the size of a memory block in the direction of the bit line (or the length in the first direction) is almost equal to the size, in the gate length direction (or the length in the first direction), of an element region AA in which a MOS transistor **43** is formed. Alternatively, the size of a memory block (or the length in the first direction) is made less than twice the length, in the first direction, of the element region AA.

(3) Problem

When the local self-boost method is used in a NAND flash memory miniaturized as described above, a problem arises: the transfer capability of MOS transistor **43** decreases.

Specifically, although not shown in FIG. **5**, a plurality of MOS transistors **43** are also arranged in the first direction. The memory block size becomes almost equal to the size of MOS transistor **43**, with the result that the distance between adjacent MOS transistors **43** in the first direction becomes smaller.

It therefore becomes difficult to place the metal wiring layer **101** connecting MOS transistor **43** located far away from memory cell array **10** to a word line WL in a space between MOS transistors **43** in the first direction. Therefore, it is necessary to cause the metal wiring layer **101** to pass over MOS transistor **43** located near memory cell array **10**.

In a case where the local self-boost method is used, when data is written, any one of the metal wiring layers **101** transfers voltage VISO. Voltage VISO is a low voltage, such as 0 V. When the metal wiring layer **101** transferring such a voltage passes over the impurity diffused layer **112** of MOS transistor **43**, the impurity diffused layer **112** might be depleted. If the impurity diffused layer **112** has been depleted, its resistance value increases. As a result, the voltage transfer capability of MOS transistor **43** decreases.

This problem is particularly serious in MOS transistor **43** that transfers voltage VPGM. If voltage VPGM is not transferred sufficiently to the word lines WL, the word lines are written erroneously (or the "0" program cannot be written).

(4) First Embodiment

In the configuration of the first embodiment, when attention is focused on a certain word line WLi, metal wiring layers **101**-(*i*+1) to **101**-(*i*+M) in the first level layer connected to an M number of word lines WL(i+1) to WL(i+M) close to word line WLi on the source side (or SGS side) are arranged as follows. Metal wiring layers **101**-(*i*+1) to **101**-(*i*+M) are arranged so as to pass through the region above the gate electrode **100** without passing over the impurity diffused layer **112**, when passing over MOS transistor **43**-*i* that transfers a voltage to word line WLi.

Accordingly, when voltage VPGM is applied to word line WLi, metal wiring layer **101**, which transfers voltage VISO, passes over gate electrode **100** without passing over impurity diffused layer **112**, above MOS transistor **43**-*i*. Therefore, metal wiring layer **101** transferring voltage VISO is prevented from adversely affecting impurity diffused layer **112** of MOS transistor **43**-*i*. That is, metal wiring layer **101** can prevent impurity diffused layer **112** from being depleted and the voltage transfer capability of MOS transistor **43**-*i* from decreasing.

This will be explained with reference to FIG. **8**. FIG. **8** is a plan view of MOS transistors **43**-*i* to **43**-(*i*+M).

As shown in FIG. **8**, MOS transistor **43**-*i* transfers voltage VPGM to word line WLi. In this case, the word line WL to which voltage VISO is applied is any one of word lines WL(i+1) to WL(i+M). Any one of metal wiring layer **101**-(*i*+1) to **101**-(*i*+M) transfers voltage VISO. FIG. **8** shows a case where voltage VISO is applied to word line WL(i+1). In the layout of the first embodiment, metal wiring layers **101**-(*i*+1) to **101**-(*i*+M) pass over MOS transistor **43**-*i*.

In the first embodiment, when metal wiring layers **101**-(*i*+1) to **101**-(*i*+M) pass over MOS transistor **43**-*i*, they pass over gate electrode **100** without passing over impurity diffused layer **112**. Accordingly, even when any one of metal wiring layer **101**-(*i*+1) to **101**-(*i*+M) transfers voltage VISO, the impurity diffused layer **112** of MOS transistor **43**-*i* transferring voltage VPGM can be prevented from being depleted.

First Modification of First Embodiment

In the NAND flash memory, VISO can be applied to not only an M number of unselected word lines closer to the source (or SGS side) than the selected word line WL but also an M number of unselected word lines on the drain side (or SGD side).

In the layout of FIG. **5**, metal wiring layers **101-0** to **101**-(*i*−1) connected to word lines WL**0** to WL(i−1) closer to the drain than the selected word line WLi do not pass over MOS transistor **43**-*i*. Accordingly, there is no need to take these wiring lines into account.

However, when metal wiring layers **101-0** to **101**-(*i*−1) pass over MOS transistor **43**-*i*, the wiring layers can be laid out as in the first embodiment. This example is shown in FIG. **9**. FIG. **9** is a plan view of MOS transistors **43**-*i* to **43**-(*i*+M) according to a first modification of the first embodiment, showing a case where MOS transistor **43**-*i* transfers voltage VPGM and MOS transistor **43**-(*i*+M) transfers voltage VISO. In FIG. **9**, the shaded regions are metal wiring lines that transfer voltage VPGM or voltage VISO.

As shown in FIG. **9**, MOS transistors **43-0** to **43**-*n* are arranged, starting from the one farthest away from memory cell array **10**. That is, MOS transistor **43**-*n* is located closest to memory cell array **10** and MOS transistor **43-0** is located farthest away from memory cell array **10**. Accordingly, in this layout, metal wiring layers **101-0** to **101**-(*i*−1) pass over MOS transistor **43**-*i*.

Therefore, in this case, metal wiring layers **101**-(*i*+M) to **101**-(*i*−1) in the first level layer connected to an M number of word lines WL(i+M) to WL(i−1) close to word line WLi on the drain side are arranged as follows. When metal wiring layers **101**-(*i*+M) to **101**-(*i*−1) are arranged so as to pass through a region above gate electrode **100** without passing over impurity diffused layer **112**, they pass over MOS transistor **43**-*i*. With this arrangement, even when any one of metal wiring layers **101**-(*i*+M) to **101**-(*i*−1) transfers voltage VISO, they do not pass over impurity diffused layer **112** of MOS transistor **43**-*i* transferring voltage VPGM, which prevents impurity diffused layer **112** from being depleted.

Furthermore, in the layout of FIG. **9**, metal wiring layers **101**-(*i*+1) to **101**-*n* connected to word lines WL(i+1) to WLn closer to the source than the selected word line WLi do not pass over MOS transistor **43**-*i*. Accordingly, there is no need to take these wiring lines into account.

Second Modification of First Embodiment

In FIGS. **5** and **9**, MOS transistors **43-0** to **43**-*n* have been arranged sequentially in the second direction in row decoder **40**. However, MOS transistors **43-0** to **43**-*n* are not necessarily arranged sequentially.

A layout in such a case will be explained with reference to FIG. **10**. FIG. **10** is a plan view of MOS transistors **43**-(*i*+M) to **43**-(*i*+M) according to a second modification of the first embodiment, showing a case where MOS transistor **43**-*i* transfers voltage VPGM and MOS transistor **43**-(*i*+M) transfers voltage VISO. In FIG. **10**, the shaded regions are metal wiring lines that transfer either voltage VPGM or VISO.

As shown in FIG. **10**, MOS transistors **43-0** to **43**-(*i*−1), **43**-(*i*+1) to **43**-(*i*+M) are arranged farther away from memory cell array **10** than MOS transistor **43**-*i*. That is, metal wiring layers **101**-(*i*+M) to **101**-(*i*−1), **101**-(*i*+1) to **101**-(*i*+M) pass over MOS transistor **43**-*i*.

In such a case, all of metal wiring layers **101**-(*i*-M) to **101**-(*i*−1), **101**-(*i*+1) to **101**-(*i*+M) are laid out as in the first embodiment. That is, metal wiring layers **1-1**(*i*+M) to **101**-(*i*−1), **101**-(*i*+1) to **101**-(*i*+M) are arranged so as to pass through a region above gate electrode **100** without passing over impurity diffused layer **112**, when they pass over MOS transistor **43**-*i*. Accordingly, even when any one of metal wiring layers **101**(*i*+M) to **101**-(*i*−1), **101**-(*i*+1) to **101**-(*i*+M) transfers voltage VISO, it does not pass over impurity diffused layer **112** of MOS transistor **43**-*i* transferring voltage VPGM, which prevents impurity diffused layer **112** from being depleted.

In other words, in the configuration where voltage VISO can be applied to an M number of unselected word lines WL adjacent to the selected word line WLi, even if J lines (j is a natural number) of the M number of unselected word lines WL are located closer to the source line than the selected word line WLi and the remaining K lines (K=M−J) are located on the bit line side, the first embodiment can be applied.

Second Embodiment

Next, a semiconductor memory device according to a second embodiment of the invention will be explained. The second embodiment is such that any one of an M number of metal wiring layers **101** is provided on impurity diffused layer **112** in the first embodiment to locate the metal wiring layer in a region where no problem will arise even if the layer is depleted. Hereinafter, only parts that differ from the first embodiment will be explained.

In row decoder **40** according to the second embodiment, when attention is focused on a certain word line WLi, at least one of metal wiring layers **101**-(*i*+1) to **101**-(*i*+M) in the first level layer connected to an M number of word lines WL(i+1) to WL(i+M) closer to the source (or SGS side) than word line WLi is arranged as follows. At least one of metal wiring layers **101**-(*i*+1) to **101**-(*i*+M) is arranged so as to pass over impurity diffused layer **112** and outside contact plug CP**10** in the element region AA when passing over MOS transistor **43**-*i* that transfers a voltage to word line WLi. That is, at least one of metal wiring layers **101**-(*i*+1) to **101**-(*i*+M) is arranged so as to be on impurity diffused layer **112** of MOS transistor **43**-*i* and face gate electrode **100**, with contact plug CP **10** intervening therebetween.

FIG. **11** is a plan view of a region where MOS transistors **43** are formed in row decoder **40** of the second embodiment, showing a case where metal wiring layer **101**-(*i*+1) is laid out as described above. FIG. **12** is a sectional view taken along line **12-12** of FIG. **11**. As shown in FIG. **11**, metal wiring layer **101**-(*i*+1) passes through a region outside contact plug CP**10** on impurity diffused layer **112** of MOS transistor **43**-*i*.

<Effect>

The configuration of the second embodiment can also prevent the voltage transfer capability of MOS transistor **43** from decreasing and produce the same effect as that of the first embodiment. The effect will be explained below.

FIG. **13** shows an equivalent circuit of MOS transistor **43** when metal wiring layer **101** transferring voltage VISO is on the MOS transistor **43** and passes through a region between contact plug CP**10** (or CP**11**) and gate electrode **100**.

As shown in FIG. **13**, the region between contact plug CP**10** (or CP**11**) and gate electrode **100** corresponds to the current path from a signal line CG to a word line WL. Accordingly, when depletion has occurred as a result of metal wiring layer **101** passing over the region, the resistance value of the current path increases. That is, a large voltage drop occurs between node N**1** and node N**2** in FIG. **13**, making it impossible to transfer a sufficient voltage to the word line WL.

With the configuration of the second embodiment, however, metal wiring layer **101** transferring voltage VISO is on the MOS transistor **43** and passes outside contact plug CP**10** (or CP**11**). FIG. **14** shows an equivalent circuit of MOS transistor **43** in this case. As shown in FIG. **14**, the region outside contact plug CP**10** (or CP**11**) has no function as a current path between the signal line CG to word line WL. Accordingly, even if the resistance value of the region increases, the effect on voltage transfer can be neglected. Therefore, the transfer capability of MOS transistor **43** can be secured sufficiently.

The second embodiment can be applied to FIGS. **9** and **10** explained in the first and second modifications of the first embodiment. Specifically, in FIG. **9**, any one of metal wiring layers **101**-(*i*+M) to **101**-(*i*−1) may be caused to pass over impurity diffused layer **112** of MOS transistor **43**-*i* and outside contact plug CP**10** (or CP**11**). Moreover, in FIG. **10**, either metal wiring layers **101**-(*i*+M) to **101**-(*i*−1) or **101**-(*i*+1) to **101**-(*i*+M) may be caused to pass over impurity diffused layer **112** of MOS transistor **43**-*i* and outside contact plug CP**10** (or CP**11**).

Third Embodiment

Next, a semiconductor memory device according to a third embodiment of the invention will be explained. The third embodiment is such that a metal wiring layer in the second level layer is used as any one of an M number of metal wiring layers **101** in the first embodiment. Hereinafter, only parts that differ from the first embodiment will be explained.

In row decoder **40** according to the third embodiment, when attention is focused on a certain word line WLi, at least one of metal wiring layers **101**-(*i*+1) to **101**-(*i*+M) connected to an M number of word lines WL(i+1) to WL(i+M) close to word line WLi on the source side (or SGS side) is caused to pass over MOS transistor **43**-*i* that transfers a voltage to word line WLi by a metal wiring layer **120** in the second layer. In this case, metal wiring layer **120** passes over impurity diffused layer **112** of MOS transistor **43**-*i*.

FIG. **15** is a plan view of a region where MOS transistors **43** are formed in row decoder **40** of the third embodiment, showing a case where metal wiring layer **101**-(*i*+1) is laid out as described above. FIG. **16** is a sectional view taken along line **16**-**16** of FIG. **15**.

As shown in FIG. **15** and FIG. **16**, metal wiring layer **101**-(*i*+1) is drawn from an element region AA onto an element isolating region STI and then is connected to metal wiring layer **120** in the second level layer via a contact plug CP**15**. Metal wiring layer **120**, which has a strip form extending in the second direction, passes over MOS transistors **43**-*i* to **43**-**0** and is drawn to the boundary between memory cell array **10** and row decoder **40**. Then, metal wiring layer **120** is connected to word line WL(i+1). In this case, metal wiring layer **120** passes over the impurity diffused layers of MOS transistors **43**-*i* to **43**-**0**.

<Effect>

The configuration of the third embodiment can also prevent the voltage transfer capability of MOS transistor **43** from decreasing, and produce the same effect as that of the first embodiment. The effect will be explained below.

In the third embodiment, metal wiring layer **120** that transfers voltage VISO is second level wiring layer. Accordingly, as shown in FIG. **16**, metal wiring layer **120** is separated from the surface of impurity diffused layer **12** by the sum of the film thicknesses of interlayer insulating film **114** and interlayer insulating film **121**. Accordingly, even when metal wiring layer **120** transfers voltage VISO, the change of impurity diffused layer **112** into a depletion layer is suppressed. Therefore, the transfer capability of MOS transistor **43** can be secured sufficiently.

The third embodiment can be applied to FIGS. **9** and **10** explained in the first and second modifications of the first embodiment. Specifically, in FIG. **9**, any one of metal wiring layers **101**-(*i*+M) to **101**-(*i*−1) may be passed over impurity diffused layer **112** of MOS transistor **43**-*i* by the second level metal wiring layer **120**. Moreover, in FIG. **10**, either metal wiring layers **101**-(*i*+M) to **101**-(*i*−1) or **101**-(*i*+1) to **101**-(*i*+M) may be passed over impurity diffused layer **112** of MOS transistor **43**-*i* by the second level metal wiring layer **120**.

As described above, in a semiconductor memory device according to each of the first to third embodiments, MOS transistors **43** in row decoder **40** are arranged as described below. In the region above transfer transistor **43**-*i* that transfers a voltage to word line WLi, an M number of word lines (M<N) close to an i-th word line WLi are arranged in any one of the following manners:

(1) The word lines are passed through a region above gate electrode **100** by a first level interconnection **101** without being passed through impurity diffused layer **112**.

(2) The word lines are passed over impurity diffused layer **112** and through a region facing to gate electrode **100** with either the first contact plug CP**10** or second contact plug CP**11** intervening therebetween, by a first level interconnection **101**.

(3) The word lines are passed over MOS transistor **43**-*i* by a second level or more interconnection **120** which is located above the first level interconnection **101**.

With this arrangement, impurity diffused layer **112** of MOS transistor **43** that transfers voltage VPGM can be prevented from having a higher resistance, and the operation reliability of the NAND flash memory can be improved.

In the second embodiment, metal wiring layer **101**-(*i*−1) has passed outside contact plug CP**10** on MOS transistor **43**-*i* (see FIG. **11**). However, metal wiring layer **101**-(*i*−1) may pass outside contact plug CP**11**, depending on layout.

In the third embodiment, metal wiring layer **120** is not necessarily passed over impurity diffused layer **112** and may be passed over gate electrode **100**. Moreover, metal wiring layer **120** can be third level interconnection or more.

Furthermore, in the second and third embodiments, one of an M number of word lines adjacent to word line WLi has passed outside contact plug CP**10** or by second level interconnection **120**. However, all of the M number of word lines may pass outside contact plug CP**10** or by the second level interconnection **120**.

In addition, the first to third embodiments may be combined suitably. Specifically, by combining the second and third embodiments, part of the M number of word lines adjacent to word line WLi may pass outside contact plug CP**10** and the remaining ones may pass by the second level interconnection **120**. Moreover, by combining the first and third embodiments, part of the M number of word lines adjacent to word line WLi may pass over gate electrode **100**, another part may pass outside contact plug CP**10**, and the remaining ones may pass by the second level interconnection **120**. Furthermore, not only the M number of word lines adjacent to word line WLi but also all the word lines WL passing over MOS transistor **34**-*i* may be laid out as explained in the first to third embodiments.

While in the above embodiments voltage VISO has been 0 V, voltage VISO is not limited to 0 V. For instance, voltage VISO may be a positive voltage or a negative voltage, provided that voltage VISO can turn off the memory cell transistors MT. In addition, the memory cell transistors MT may have a MONOS structure where the charge accumulation layer **84** is formed by an insulating film instead of a conducting film.

Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details and representative embodiments shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.

What is claimed is:

1. A semiconductor memory device, comprising:
   a memory cell unit including a first memory cell, a second memory cell, a third memory cell, and a fourth memory cell that are connected in series;
   a first word line connected to the first memory cell;
   a second word line connected to the second memory cell;
   a third word line connected to the third memory cell;
   a fourth word line connected to the fourth memory cell;
   a driver circuit configured to apply a voltage to the first memory cell, the second memory cell, the third memory cell, and the fourth memory cell; and
   a first transistor including a first diffused layer and a second diffused layer, wherein the first diffused layer is connected to the first word line, and the second diffused layer is connected to the driver circuit,
   wherein when data is written into the first memory cell, a first voltage is applied to the first word line, a second voltage is applied to the second word line and the third word line, and a third voltage is applied to the fourth word line, and
   the first voltage is larger than both the second voltage and the third voltage, and the third voltage is larger than the second voltage, and
   wherein the second memory cell and the third memory cell are located between the first memory cell and the fourth memory cell, and
   the second word line and the third word line are located above a gate electrode of the first transistor without passing over the first diffused layer and the second diffused layer of the first transistor.

2. The device according to claim 1, further comprising:
   a second transistor connected between the second word line and the driver circuit;
   a third transistor connected between the third word line and the driver circuit; and
   a fourth transistor connected between the fourth word line and the driver circuit,
   wherein each of the first word line, the second word line, the third word line, and the fourth word line is arranged in a first direction,
   each of the first transistor, the second transistor, the third transistor, and the fourth transistor has a gate length in a second direction perpendicular to the first direction, and
   the first transistor, the second transistor, the third transistor, and the fourth transistor are arranged in the first direction.

3. The device according to claim 2, wherein the first memory cell, the second memory cell, the third memory cell, and the fourth memory cell are connected between a first selection transistor and a second selection transistor, and
   the memory cell unit is connected to a bit line via the first selection transistor, and is connected to a source line via the second selection transistor, and
   wherein a distance between the first transistor and the memory cell unit is smaller than a distance between the second transistor and the memory cell unit.

4. The device according to claim 3, wherein the second memory cell, the third memory cell, and the fourth memory cell are located between the first memory cell and the second selection transistor.

5. The device according to claim 1, wherein the second voltage turns off the second memory cell and the third memory cell regardless of held data.

6. The device according to claim 1, further comprising a contact plug formed on the second diffused layer,
   wherein the first transistor is connected to the driver circuit via the contact plug, and
   the fourth word line is located in a region above the second diffused layer and between a gate electrode of the first transistor and the contact plug.

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